# N-Channel Enhancement Mode Field Effect Transistor

- **Features**

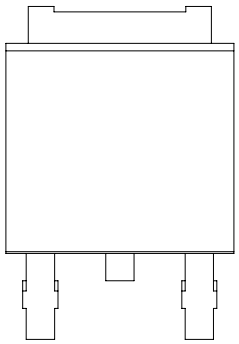
$V_{DS}$ 60V，$V_{GS}$ 20V, $I_D$ 18A，

$R_{DS(ON)}$ ＜40mΩ @$V_{GS}$= 10V

- **General Description**

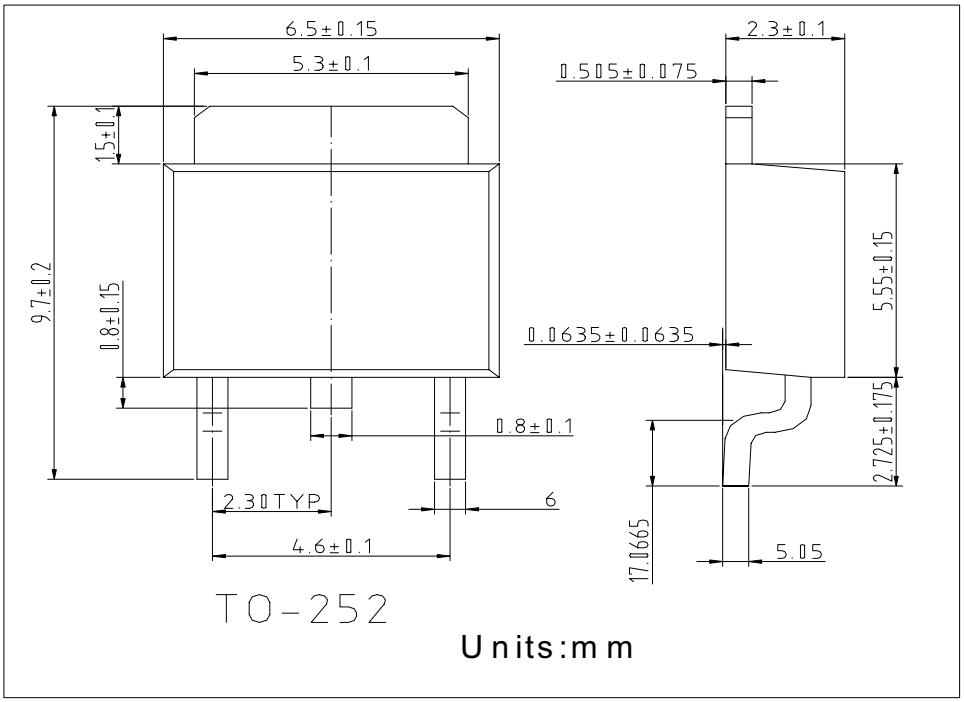
This device has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

- **Pin Configurations**



G D S

- **Package Information**



- **Absolute Maximum Ratings** @$T_A$=25℃ unless otherwise noted

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 60 | V |
| Gate-Source Voltage | $V_{GSS}$ | ±20 | V |
| Maximum Drain Current - Continuous | $I_D$ | 18 | A |
| - Pulsed | | 45 | |
| Continuous Power Dissipation(large heatsick) | $P_D$ | 110 | W |
| Operating and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 to 150 | ℃ |

- **Electrical Characteristics** @$T_A$=25℃ unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 60 | -- | -- | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | -- | -- | 1 | μA |
| Gate - Body Leakage | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | -- | -- | ±100 | nA |
| **ON CHARACTERISTICS[b]** | | | | | | |
| Gate Threshold Voltage | $V_{GS\ (th)}$ | $V_{DS}$ = VGS, $I_D$ = 250 μA | 1.1 | 1.5 | 2.9 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 10 V, $I_D$ = 10 A | -- | 35 | 40 | mR |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 5 A | -- | 42 | 50 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 15 V, $I_D$ = 10 A | -- | 20 | -- | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1MHz | -- | 1000 | -- | pF |
| Output Capacitance | $C_{oss}$ | | -- | 200 | -- | |
| Reverse Transfer Capacitance | $C_{rss}$ | | -- | 100 | -- | |
| **SWITCHING CHARACTERISTICS[b]** | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DS}$ = 30 V, $I_D$ = 10 A, $V_{GS}$ = 10 V, $R_{gen}$ =4.7Ω | -- | 45 | | ns |
| Turn-On Rise Time | $t_r$ | | -- | 22 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | -- | 42 | | |
| Turn-Off Fall Time | $t_f$ | | -- | 13 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 48 V, $I_D$ = 18 A, $V_{GS}$ = 10 V | -- | 50 | | nC |
| Gate–Source Charge | $Q_{gs}$ | | -- | 20 | -- | |
| Gate–Drain Charge | $Q_{gd}$ | | -- | 15 | -- | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS[b]** | | | | | | |
| Drain–Source Diode Forward Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 18 A [(2)] | -- | -- | 1.3 | V |

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

- **Typical Performance Characteristics**

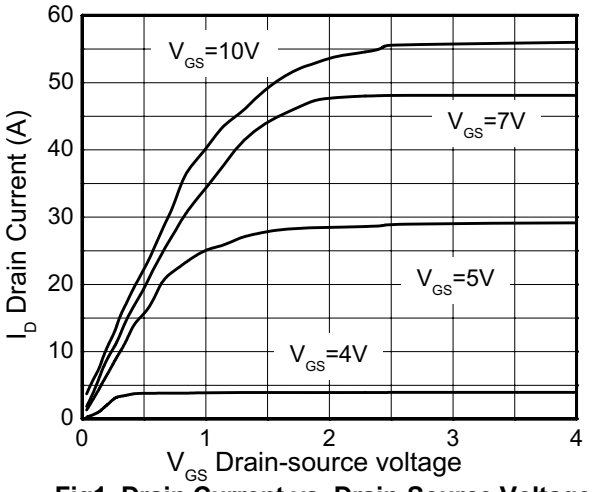



**Fig1. Drain Current vs. Drain-Source Voltage**

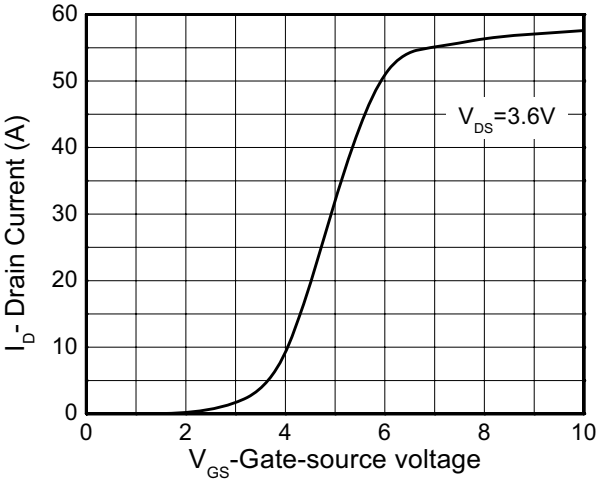



**Fig2. Drain Current vs. Gate-Source Voltage**

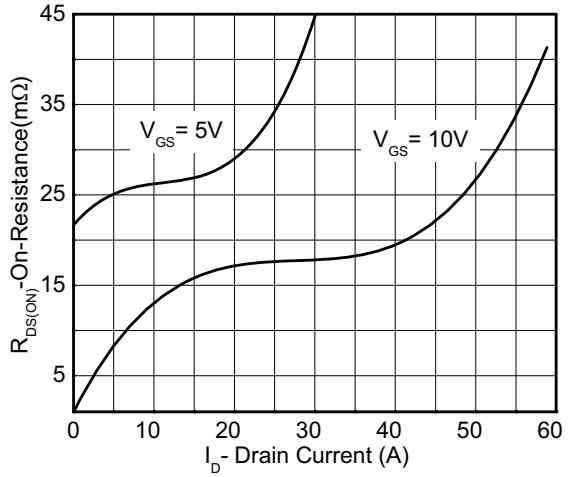



**Fig3. On-Resistance vs. Drain Current**

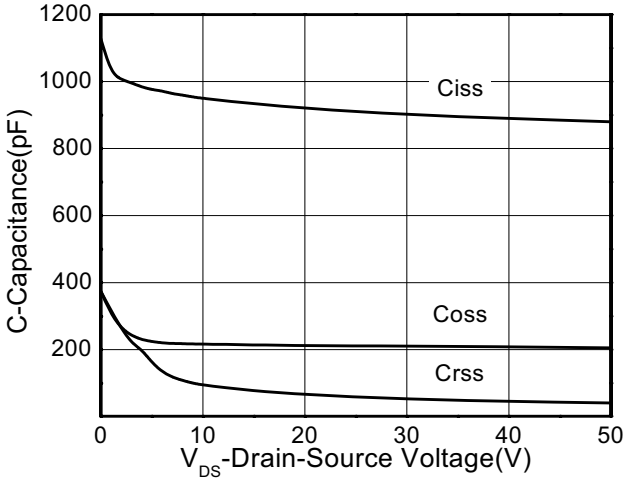



**Fig4. Drain-Source Voltage vs.Capacitance**

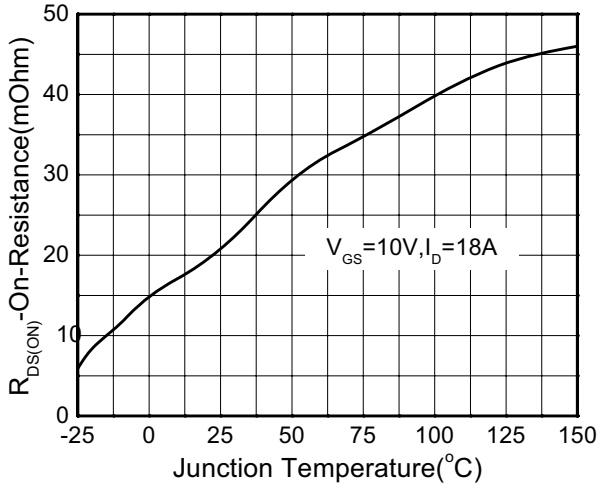



**Fig5. On-Resistance vs. Junction Temperature**

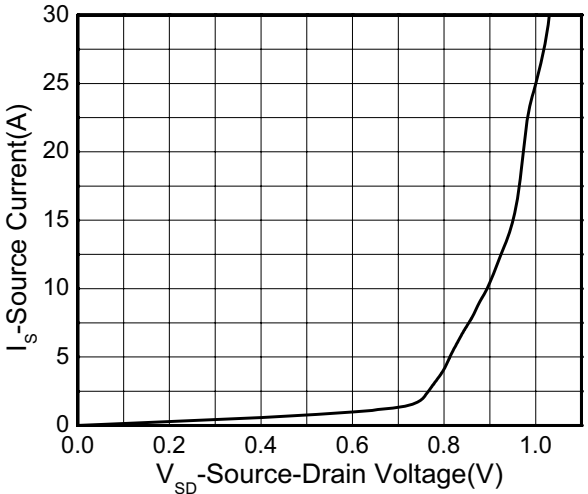



**Fig6.Body Diode Forward Voltage vs Diode Current**

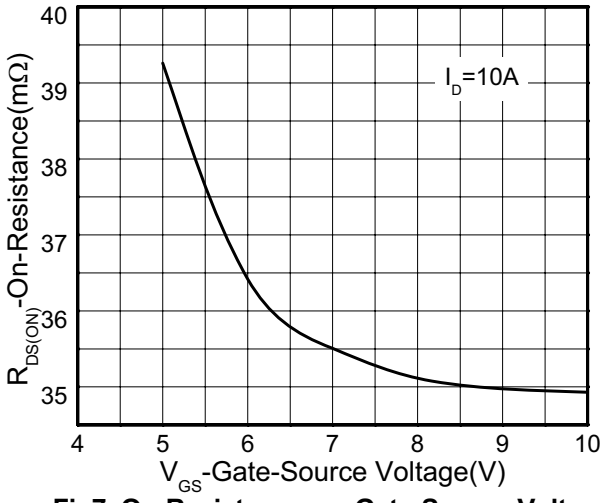



**Fig7. On-Resistance vs. Gate-Source Voltage**

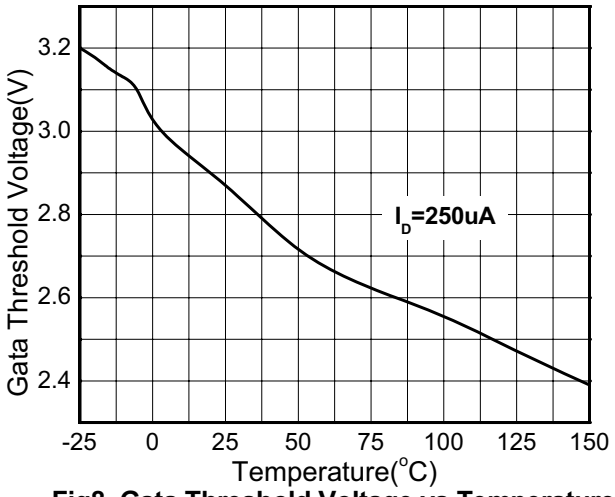



**Fig8. Gata Threshold Voltage vs Temperature**

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