PLL MOTOR SPEED CONTROL CIRCUIT FOR HI-FI APPLICATIONS

The TDA1533 is a monolithic integrated circuit intended for PLL motor speed control in several hi-fi applications; e.g. record players, cassette recorders, reel-to-reel, and operates in accordance with the phase-locked-loop (PLL) system.
The circuit incorporates the following functions:

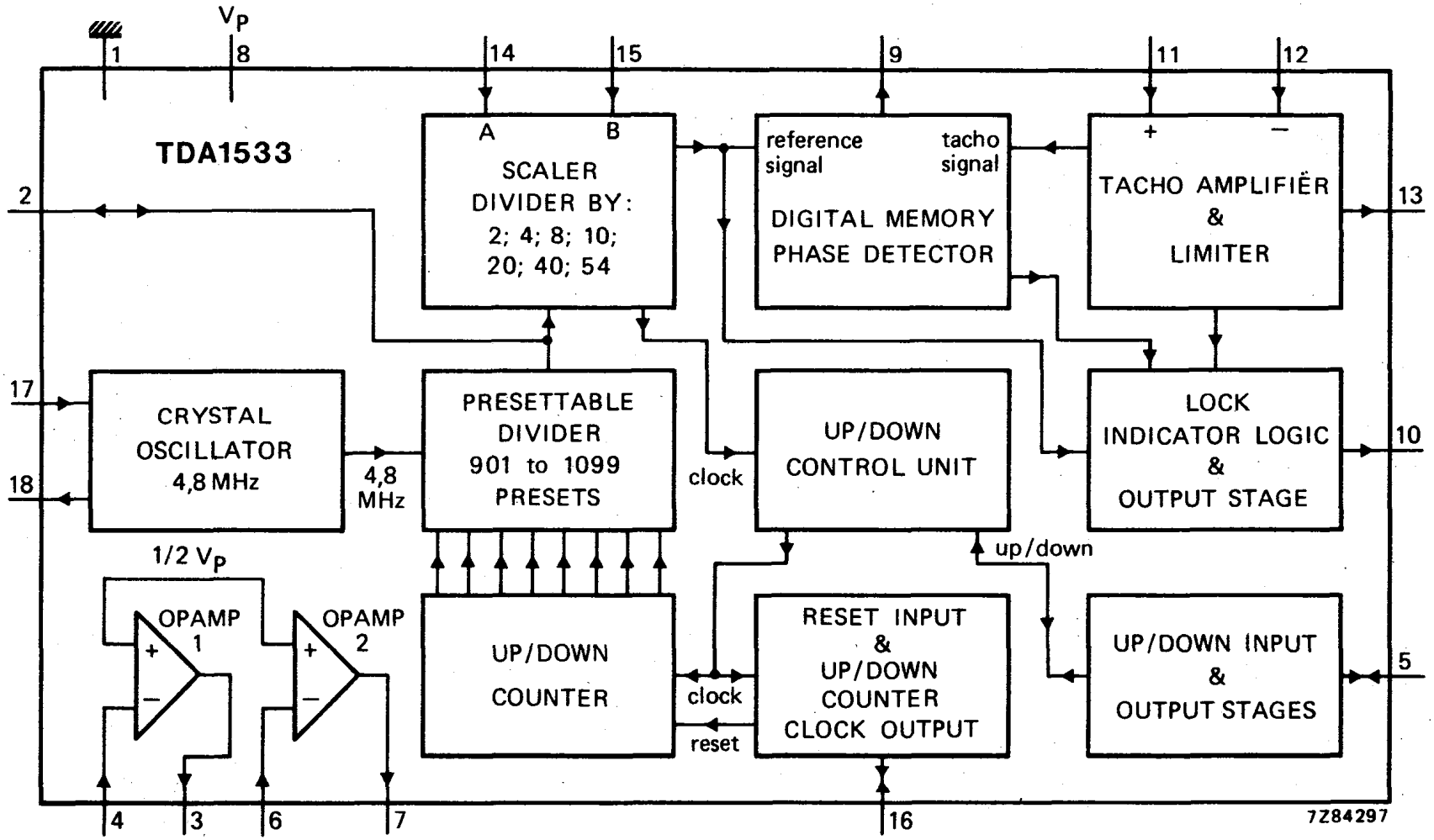
- A quartz reference oscillator
- A synthesizer for adjustment of the phase detector reference frequency
- A programmable scaler for the several applications
- A digital memory phase detector
- A tacho-signal amplifier/limiter
- Two operational amplifiers for the external integration and loop filtering of the phase detector output.

QUICK REFERENCE DATA

Supply voltage range	V_P		9 to 11	V
Supply current	I_P	typ.	50	mA
Crystal oscillator				
Frequency	f	<	5	MHz
Temperature coefficient	TC	<	$0{,}1.10^{-6}$	K^{-1}
Tacho input				
Input voltage	V_I		−0,3 to + 10	V
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10	mV
Operational amplifiers				
Voltage gain	G_v	typ.	10 000	
Input bias current	I_{bias}	<	100	nA
Input offset voltage	V_{io}	<	15	mV
Temperatures				
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		0 to + 60	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).



PINNING

1. Ground
2. Test input/output
3. Output of opamp 1
4. Input of opamp 1
5. Up/down input/output
6. Input of opamp 2
7. Output of opamp 2
8. Positive supply (+ 10 V)
9. Phase detector output
10. Lock indicator output
11. + input tacho limiter
12. – input tacho limiter
13. Output tacho limiter
14. A-input scaler control
15. B-input scaler control
16. Reset input/output
17. Crystal oscillator input
18. Crystal oscillator output

Fig. 1 Block diagram.

GENERAL DESCRIPTION (see also Fig. 1)

The crystal frequency (e.g. 4,8 MHz) is divided by the presettable 901 to 1099 divider. The scaler is used to obtain the reference signal for the digital memory phase detector. The tacho signal is derived from the tacho amplifier/limiter.

The output of the phase detector becomes HIGH on the positive-going edge of the reference signal, and it is floating on the first-coming positive edge of the tacho signal, if the angle between the edges is not more than 360°. The output becomes LOW if the first positive-going edge is the edge of the tacho signal, and it is floating on the first-coming positive edge of the reference signal. This means that the holding range is 720°.

The lock indication output is HIGH, except for the period between the two positive and the two negative-going edges of the tacho and reference signals.

The dividing number of the presettable divider depends on the state of its presets, thus on the position of the up/down counter.

A pull-up to the IC supply voltage of the reset input results into a reset of the up/down counter and dividing by 1000.

The up/down counter can be changed in position by means of the up/down input and the up/down control unit, and therefore the divisors of the presettable divider in a range from 901 to 1099.

The clock of the up/down counter is available at the reset input as a 0,1 V_P to 0,8 V_P pulse.

The timing diagram of the up/down counter is given in Fig. 2.

The up/down input and the scaler control inputs are 3-state inputs. The scaler truth table is given below.

A HIGH level at the up/down input gives an increase, a LOW level a decrease, of the phase detector reference signal frequency.

The information at the up/down input will be internally forced on the state present, over a period of 250 ms. Together with the up/down clock at the reset pin, this offers the possibility of displaying the number of clock pulses used.

SCALER TRUTH TABLE

control inputs A	control inputs B	division ratio
H	H	note 1
H	L	note 2
F	F	4
F	H	8
F	L	2
H	F	54
L	H	10
L	L	20
L	F	40

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
F = floating (pin open)

Notes

1. Test 1; general preset.
2. Test 2; fast clock via test pin (pin 2).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{8-1}$	max.	12 V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 80 °C

CHARACTERISTICS

Supply voltage	V_P	typ.	10 V
			9 to 11 V
Supply current	I_P	typ.	50 mA
Operating ambient temperature	T_{amb}		0 to 60 °C

The following characteristics are measured at V_P = 10 V; T_{amb} = 25 °C; unless otherwise specified

Crystal oscillator

Frequency	f	typ.	4,8 MHz
		<	5,0 MHz
Input voltage HIGH	V_{IH}		2,6 to 10 V
Input voltage LOW	V_{IL}		−2,0 to + 2,0 V
Input resistance	R_i	>	50 kΩ
Input capacitance	C_i	<	5 pF
Open voltage 1	V_{o1}	typ.	2 V
Open voltage 2	V_{o2}	typ.	1,3 V
Temperature coefficient	TC	<	$0{,}1.10^{-6}$ K^{-1}

Lock indicator output (open collector)

Output voltage HIGH	V_{OH}	<	12 V
Output voltage LOW at 10 mA	V_{OL}	typ.	0,25 V
		<	0,5 V
Output sink current	I_o	typ.	10 mA
		<	20 mA

Phase detector output

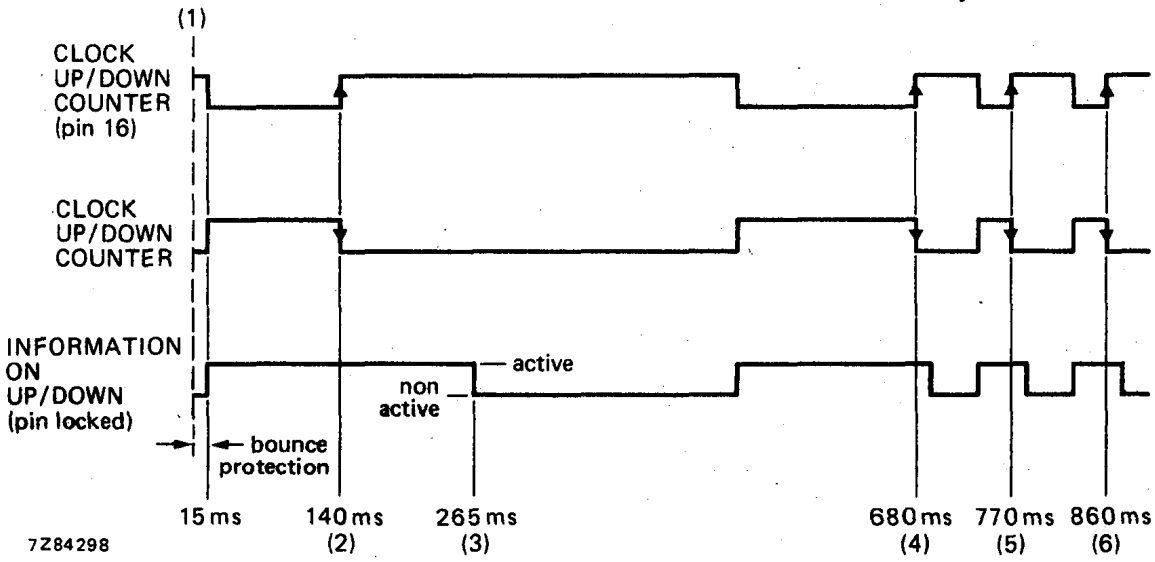
Output voltage HIGH at 20 μA	V_{OH}	>	9,5 V
		typ.	9,7 V
Output voltage LOW at 20 μA	V_{OL}	typ.	0,3 V
		<	0,5 V
Output current			
source	I_o	>	30 μA
		typ.	44 μA
sink	I_o	>	30 μA
		typ.	30 μA

Tacho input			
Input voltage	V_I		−0,3 to + 10 V
Input biasing current	I_{bias}	typ. <	0,5 μA 5,0 μA
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10 mV
Offset voltage over temperature range	V_{io}	typ. <	0,1 mV 2,0 mV
Offset current over temperature range	I_{io}	typ. <	50 nA 250 nA
Tacho output (open collector)			
Output voltage HIGH	V_{OH}	<	12 V
Output voltage LOW at 5 mA	V_{OL}	<	0,5 V
Output sink current	I_o	<	10 mA
Up/down - input/output			
Input voltage LOW	V_{IL}	typ. 	0 V −0,4 to + 0,4 V
Output voltage HIGH	V_{OH}		3 to 10 V
Open voltage	V_o	typ. 	0,7 V 0,6 to 0,8 V
Open voltage HIGH at 0,5 mA	V_{oH}	> typ.	8,5 V 9,0 V
Open voltage LOW at 0,5 mA	V_{oL}	<	0,5 V
Output sink current	I_o	<	10 mA
Output source impedance	$\lvert Z_o \rvert$	<	1,5 kΩ
Scaler inputs			
Input voltage LOW	V_{IL}	typ. 	0 V −0,4 to + 0,4 V
Input voltage HIGH	V_{IH}		4 to 10 V
Open voltage	V_o	typ. 	0,7 V 0,6 to 0,8 V
Reset input/output			
Input voltage HIGH	V_{IH}	> typ.	9,5 V 10,0 V
Output voltage LOW	V_{OL}	typ. <	0,3 V 0,5 V
Output voltage HIGH	V_{OH}	typ.	8 V

CHARACTERISTICS (continued)

Operational amplifiers

Voltage gain	G_v	typ.	10 000
Input bias current	I_{bias}	typ. <	30 nA 100 nA
Output sink current at V_o = 1 V	I_o	typ.	0,1 mA
Output source current at V_o = 9 V	I_o	> typ.	15 mA 20 mA
Input offset voltage	V_{io}	<	15 mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$	<	0,25 mV/K
Bandwidth (3 dB)	B		60 Hz



(1) Start operation of up/down pin.
(2) 1st clock pulse.
(3) From this point on, restart of cycle by second excitation is possible.
(4) 2nd clock pulse.
(5) 3rd clock pulse.
(6) 4th clock pulse.

Fig. 2 Timing diagram of up/down counter.