

CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

High-Voltage Types (20-Volt Rating)

■ CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

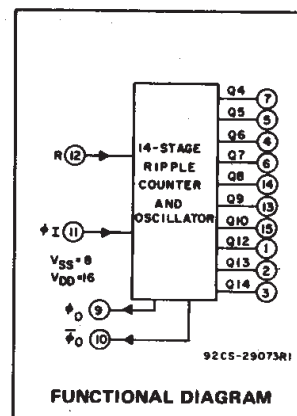
The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- 12 MHz clock rate at 15 V
- Common reset
- Fully static operation
- Buffered inputs and outputs
- Schmitt trigger input-pulse line
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"

Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration
- RC oscillator frequency of 690 kHz min. at 15 V



Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

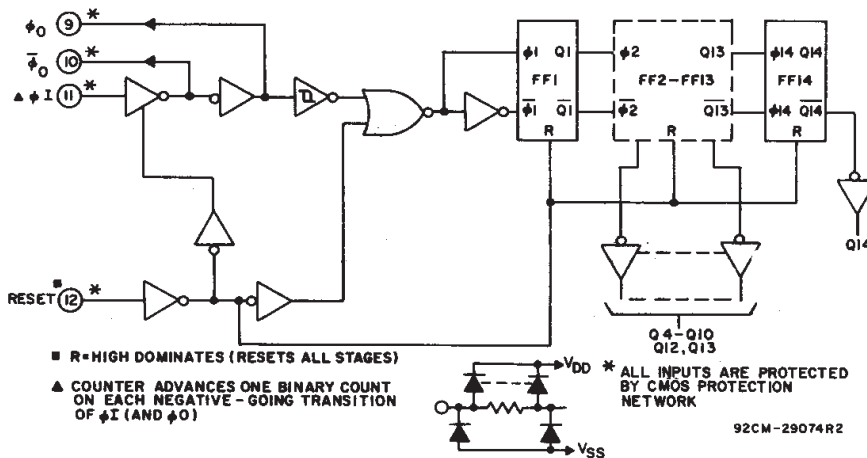


Fig. 1 - Logic diagram.

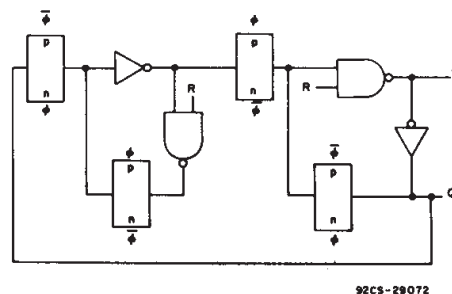


Fig. 2 - Detail of typical flip-flop stage.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} + 0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ\text{C}$

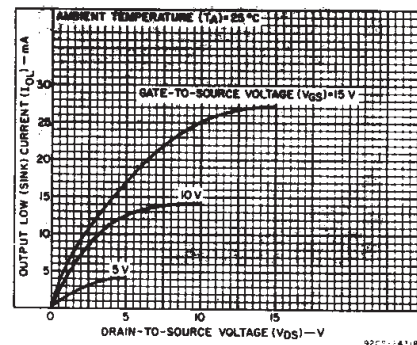


Fig. 3 - Typical n-channel output low (sink) current characteristics.

CD4060B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current*, I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current*, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

* Data not applicable to terminal 9 or 10.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD}	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	—	3	18	V
Input-Pulse Width, t_W ($f = 100$ kHz)	5 10 15	100 40 30	— — —	ns
Input-Pulse Rise Time and Fall Time, $t_{r\phi}$, $t_{f\phi}$	5 10 15	Unlimited		
Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)	5 10 15	— — —	3.5 8 12	MHz
Reset Pulse Width, t_W	5 10 15	120 60 40	— — —	ns

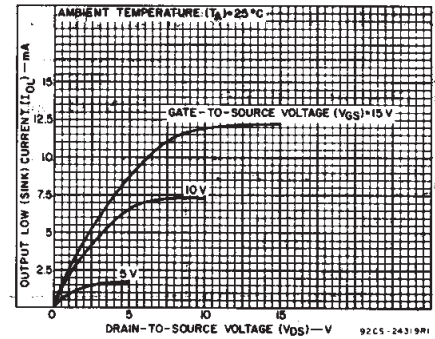


Fig. 4 — Minimum n-channel output low (sink) current characteristics.

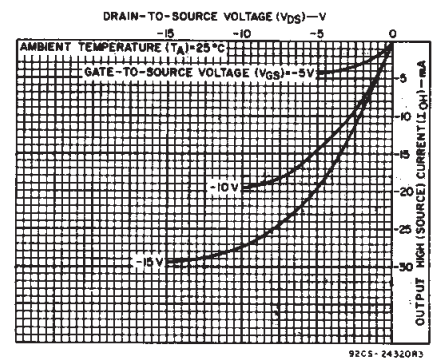


Fig. 5 — Typical p-channel output high (source) current characteristics.

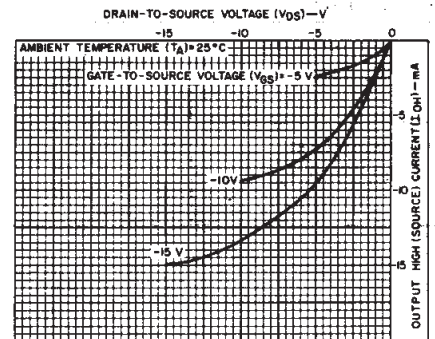


Fig. 6 — Minimum p-channel output high (source) current characteristics.

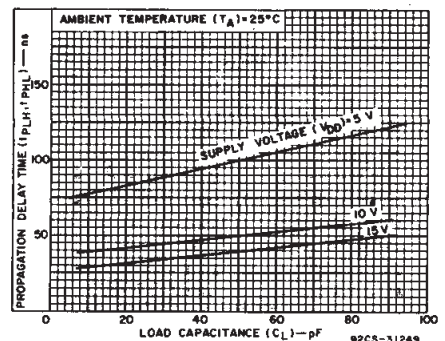


Fig. 7 — Typical propagation delay time (Q_n to Q_{n+1}) as a function of load capacitance.

CD4060B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V _{DD} (V)	MIN.	TYP.	MAX.	
Input-Pulse Operation						
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL} , t_{PLH}		5	—	370	740	ns
		10	—	150	300	
		15	—	100	200	
Propagation Delay Time, Q_n to Q_{n+1} ; t_{PHL} , t_{PLH}		5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Transition Time, t_{THL} , t_{TLH}		5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Min. Input-Pulse Width, t_W	f = 100 kHz	5	—	50	100	
		10	—	20	40	
		15	—	15	30	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			
		10				
		15				
Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)		5	3.5	7	—	MHz
		10	8	16	—	
		15	12	24	—	
Input Capacitance, C ₁	Any Input		—	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	—	180	360	ns
		10	—	80	160	
		15	—	50	100	
Minimum Reset Pulse Width, t_W		5	—	60	120	
		10	—	30	60	
		15	—	20	40	

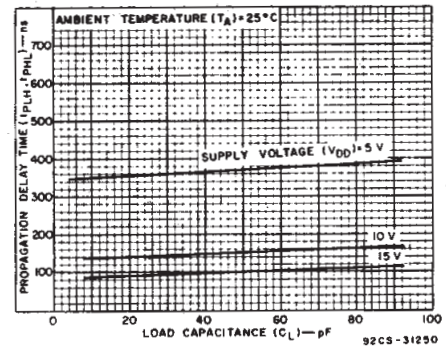


Fig. 8 — Typical propagation delay time (ϕ_I to Q4 Output) as a function of load capacitance.

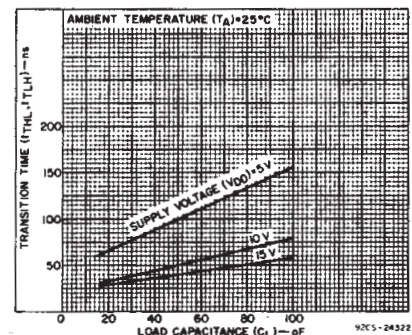


Fig. 9 — Typical transition time as a function of load capacitance.

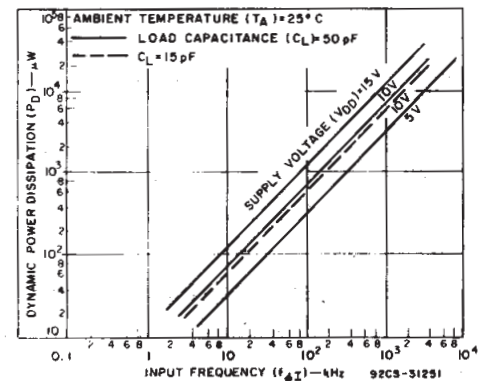


Fig. 10 — Typical dynamic power dissipation as a function of input frequency.

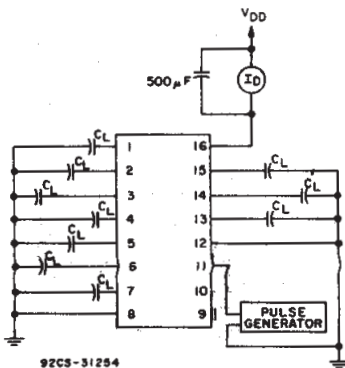


Fig. 11 — Dynamic power dissipation test circuit.

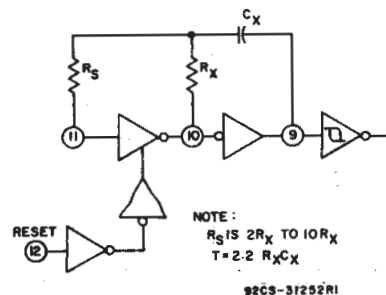


Fig. 12 — Typical RC circuit.

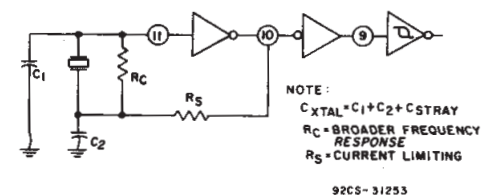


Fig. 13 — Typical crystal circuit.

CD4060B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$ [cont'd]

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS			UNITS
			Min.	Typ.	Max.	
RC Operation						
Variation of Fre- quency (Unit-to-Unit)	C _X = 200 pF, R _S = 560 kΩ, R _X = 50 kΩ	5	—	23±10%	—	kHz
		10	—	24±10%	—	
		15	—	25±10%	—	
Variation of Fre- quency with voltage change (Same Unit)	C _X = 200 pF, R _S = 560 kΩ, R _X = 50 kΩ	5V to 10 V 10V to 15V	— —	1.5 0.5	— —	
R _X max.	C _X = 10 μF = 50 μF = 10 μF	5	—	—	20	MΩ
		10	—	—	20	
		15	—	—	10	
C _X max.	R _X = 500 kΩ = 300 kΩ = 300 kΩ	5	—	—	1000	μF
		10	—	—	50	
		15	—	—	50	
Maximum Oscillator Frequency*	R _X = 5 kΩ R _S = 30 kΩ C _X = 15 pF	10	530	650	810	kHz
		15	690	800	940	
Drive Current at Pin 9 (For Oscillator Design)	I _{OL}	V _O = 0.4 V	5	0.16	0.35	mA
		= 0.5 V	10	0.42	0.8	
		= 1.5 V	15	1	2	
	I _{OH}	V _O = 4.6 V	5	-0.16	-0.35	
		= 9.5 V	10	-0.42	-0.8	
		= 13.5 V	15	-1	-2	

*RC oscillator applications are not recommended at supply voltages below 7 V for $R_X < 50 \text{ k}\Omega$.

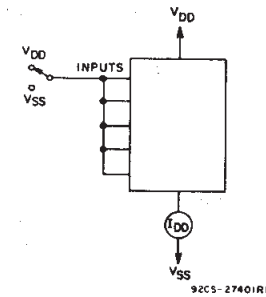


Fig. 14 - Quiescent device current.

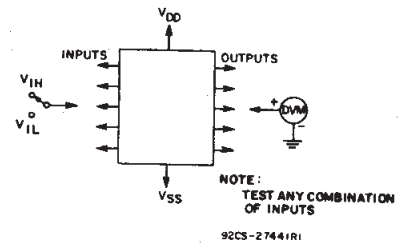


Fig. 15 - Input voltage.

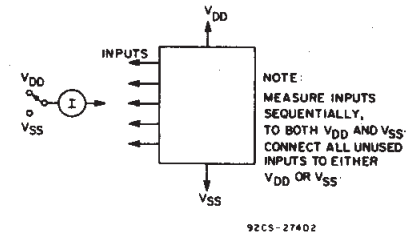
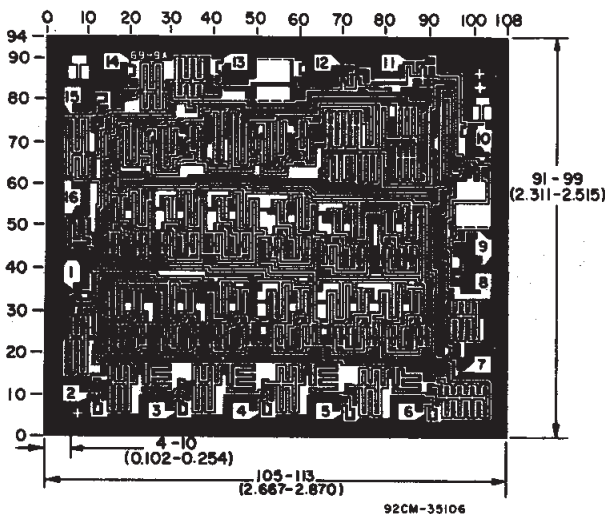
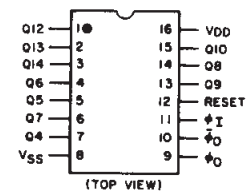


Fig. 16 - Input current.



Chip dimensions and pad layout for CD4060B

TERMINAL DIAGRAM



92CS-23761R2

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4060BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4060BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4060BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4060BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4060BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4060BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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