until the ringing amplitude has decayed down to about 15% of its initial value. This square wave is connected straight to the clock inputs of shift registers IC2a and IC2b.

**3. The LED bargraph display:** IC2 consists of a pair of identical four-bit serial-in/parallel-out shift registers, connected to form a single eight-bit unit, with each output driving one LED in the `bargraph' display via resistors R17 to R24. The serial data input of the first stage (pin 15) is permanently connected to the positive supply, or logic 1.

### One measurement

For the first 5us after the commencement of a new 2ms measuring pulse, both shift registers are reset to zeroes on all outputs, as described earlier. At the same time the initial positive pulse applied to the LOPT drives IC1b's output, connected to both shift registers' clock inputs, to a low (logic 0) level - unless the test leads are shorted.

If the LOPT primary circuit is OK, it will ring during the next several hundred microseconds. For each ring above about 15% of its initial value, it will cause a high-going pulse to be applied to the shift register clock inputs, resulting in the logic 1 on IC2 pin 15 being moved one shift register stage further along. It doesn't matter if the LOPT rings more than eight times - all LEDs will still remain illuminated.

So the overall result is that one LED illuminates for each LOPT ring cycle above 15% of the initial level, and this condition remains until the start of the next 2ms measuring pulse. Phew!

### Usage & limitations

In order to assess the usefulness of this design, we gave several prototype LOPT/FBT testers to technician friends to evaluate for many months, then asked for their comments and thoughts on how to put the tester to best use.

The first response is from Larry Sabo, an experienced monitor technician in Ottawa, Canada who also suggested the front panel layout:

*One of the first things I do to check out a monitor is connect the tester between the HOT collector and ground. If no or only a few LEDs light, I check the HOT, damper diodes and tuning caps for shorts using a DMM. If these are OK, I check for an open fusible resistor in the circuit feeding B+ to the LOPT, and for shorts/leakage in diodes on the LOPT secondaries. I also check the bypass capacitor on the DC supply to the LOPT primary for excessive ESR.*

*If these check OK, I ring the horizontal yoke with its connector unplugged. It will normally ring seven times on its own. If the yoke rings OK, I unsolder all but the LOPT primary winding and ground pins, and ring the primary. If the primary still rings low with everything else disconnected, the LOPT is probably defective.*

*Most LOPTs on their own will ring 8+ times, but some ring only four or five, even when they are perfectly normal. So it is prudent to confirm the diagnosis by ringing an identical known-good LOPT, if at all possible.*

*Sometimes an LOPT is defective, but still rings normally with the tester, e.g. due to leakage or arcing that only occurs at full operating voltage. The problem will sometimes be manifest by heavy loading of the B+ supply, spurious ringing and/or reduced voltages on the HOT*

## Parts List

**Resistors**
(All 5% 0.25W carbon)

| | |
|---|---|
| R1,2,3,14 | 1M |
| R4 | 2.2M |
| R5,16 | 47k |
| R6,7,9, R17-24 | 1k |
| R8 | 270 ohms |
| R10,15 | 4.7k |
| R11 | 33k |
| R12 | 150k |
| R13 | 10k |

**Capacitors**

| | |
|---|---|
| C1 | 100uF 16/25VW RB electrolytic |
| C2,3,5,7 | 0.047uF MKT |
| C4 | 0.01uF MKT |
| C6 | 100pF disc ceramic |

**Semiconductors**

| | |
|---|---|
| D1,2,3 | 1N914 / 1N4148 silicon diode |
| IC1 | LM393 dual comparator |
| IC2 | 4015 / MC14015 / CD4015 dual 4-bit shift register |
| LED1,2,3 | Rectangular red LED |
| LED4,5 | Rectangular yellow LED |
| LED6,7,8 | Rectangular green LED |
| Q1 | BC328 / 2N5819 PNP silicon transistor |

**Miscellaneous**
PCB, ZA1137 51 x 76mm; small (UB3) plastic case, 130 x 68 x 41mm (DSE H-2853); front panel; battery holder for 4 x AAA cells; battery snap ; power switch, push on/off; one DIP8 IC socket, one DIP16; 4 x tapped spacers; screws, nuts and washers (see Screw size and allocation guide); 1 x red, 1 x black 4mm banana sockets; test leads with 4mm banana plugs; double-sided adhesive tape; wire, PCB pins, solder and instructions.

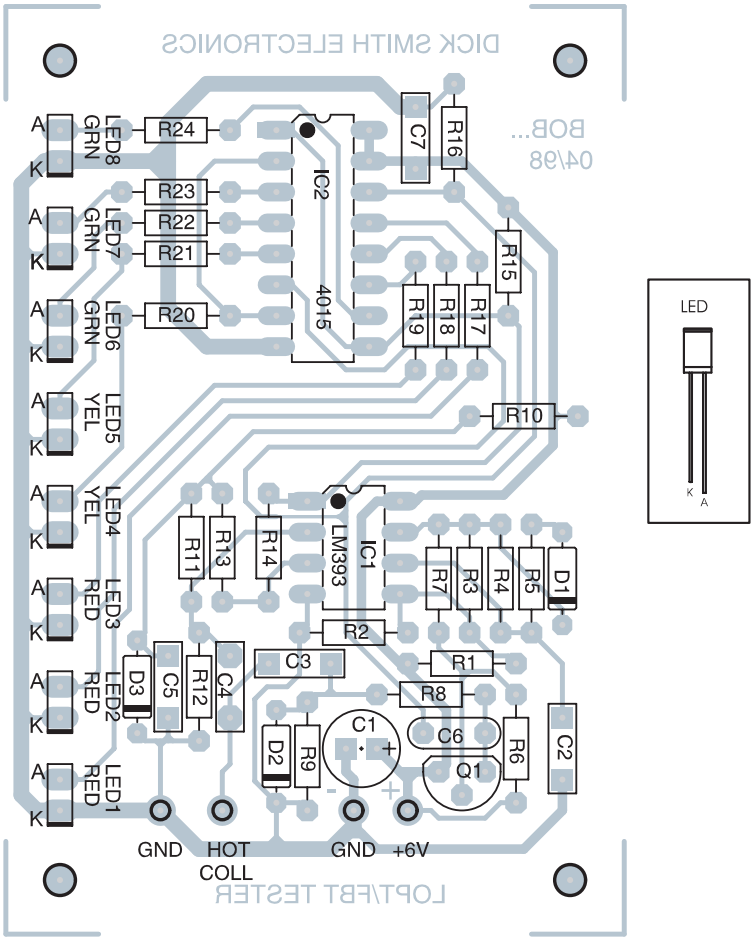


***Fig.3: Use this PCB overlay and the facing photo as a guide in assembling the tester.***